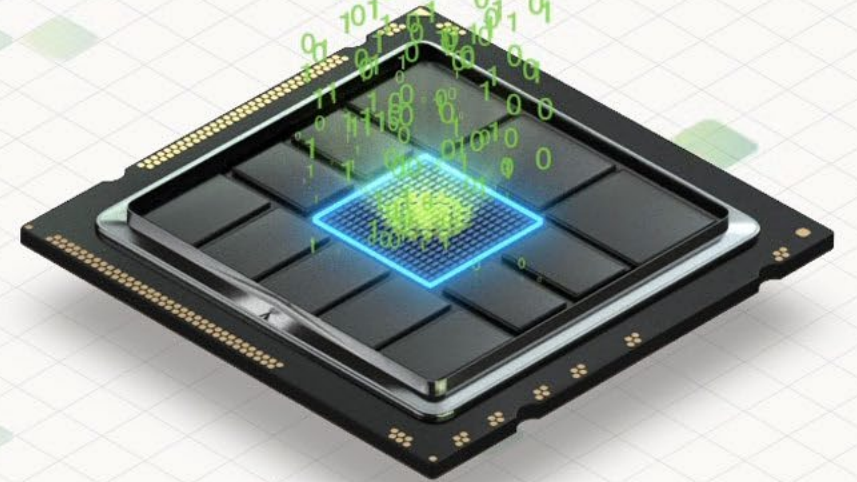


ReRAM for Energy-Efficient FD-SOI: *From Embedded Memory to Edge AI and In-Memory Computing*

Coby Hanoach, CEO, Weebit Nano
September 2026



Embedded Memory Requirements are Evolving

New applications and system trends are pushing embedded NVM to do more than ever before

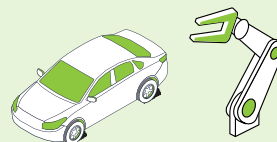
What's driving change?



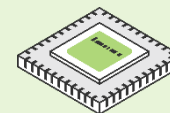
**More intelligence
at the edge**



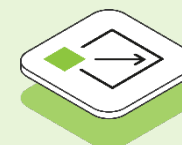
**Proliferation of smart,
connected devices**



**Growing automotive and
industrial electronics**



**More functionality
integrated into SoCs**



**Continued process
scaling**

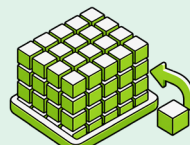
What embedded NVM must deliver



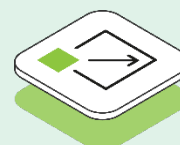
Lower power



Higher performance



Greater density



Scalability



Reliability/endurance



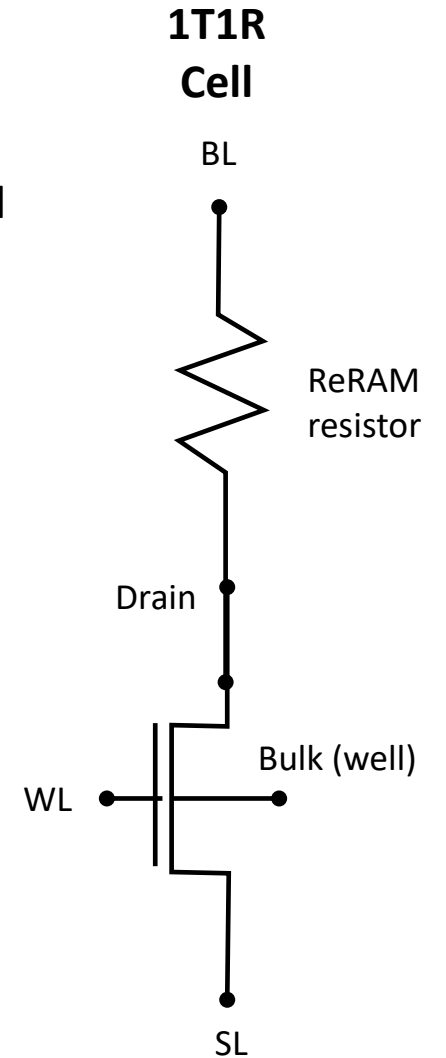
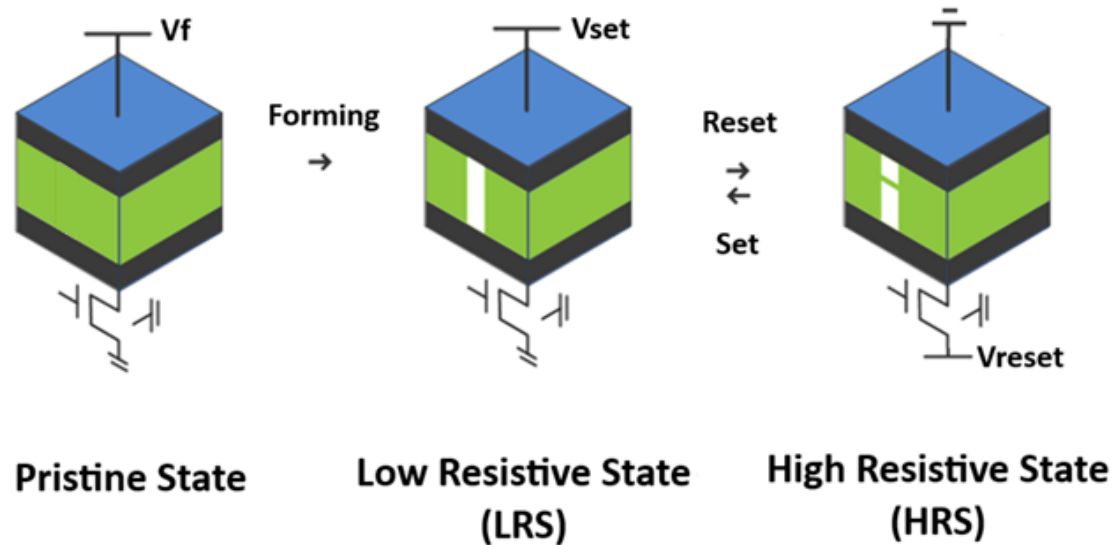
Cost efficiency

ReRAM Fundamentals

- ❖ Weebit ReRAM is based on oxygen vacancies filament (OxRAM)
 - ◆ By applying different voltage levels on the resistive layer, a filament is created or dissolved
 - **FORMING** – Initialization of the filament, done at production test
 - **SET** – Recreation of the Conductive Filament: HRS→LRS
 - **RESET** – Partial dissolution of the Conductive Filament: LRS → HRS
 - ◆ Data retained within the stack is resilient to many environmental conditions

Low Power Consumption

- ✓ Low read voltage <1V
- ✓ Low write voltage <3V
- ✓ No erase before write
- ✓ Low currents
- ✓ Zero standby power
- ✓ Fast operation



Why ReRAM?

Superior to embedded flash across key metrics



MANUFACTURING ADVANTAGE

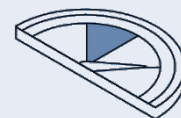
3-4x

Lower added wafer cost
vs. embedded flash

2-mask adder

(vs. ~10)

Shorter cycle time;
fewer manufacturing steps



PERFORMANCE ADVANTAGE

10x-100x

Faster program time
than embedded flash

Bit/byte addressable
No sector erase

>10x

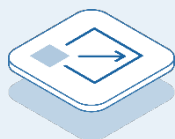
Better endurance
vs. embedded flash

Demo 100K-1M
write cycles

~100x

More energy efficient
vs. embedded flash

Low voltage, low current
write operations



SCALABILITY & INTEGRATION ADVANTAGE

<28nm

Scales to processes far
below limits of flash

Proven @ 28nm and 22nm
Scalable **below**

BEOL¹

0 interference w/ analog
& power devices

Best NVM for PMIC
& mixed-signal



RELIABILITY ADVANTAGE

150°C

Reliable for
Automotive designs

Grade-0 conditions
and profiles

~350x

Better radiation tolerance
vs. flash²

Also tolerant to EMI

Lower cost. Higher performance. Better reliability. Future-proof scalability.

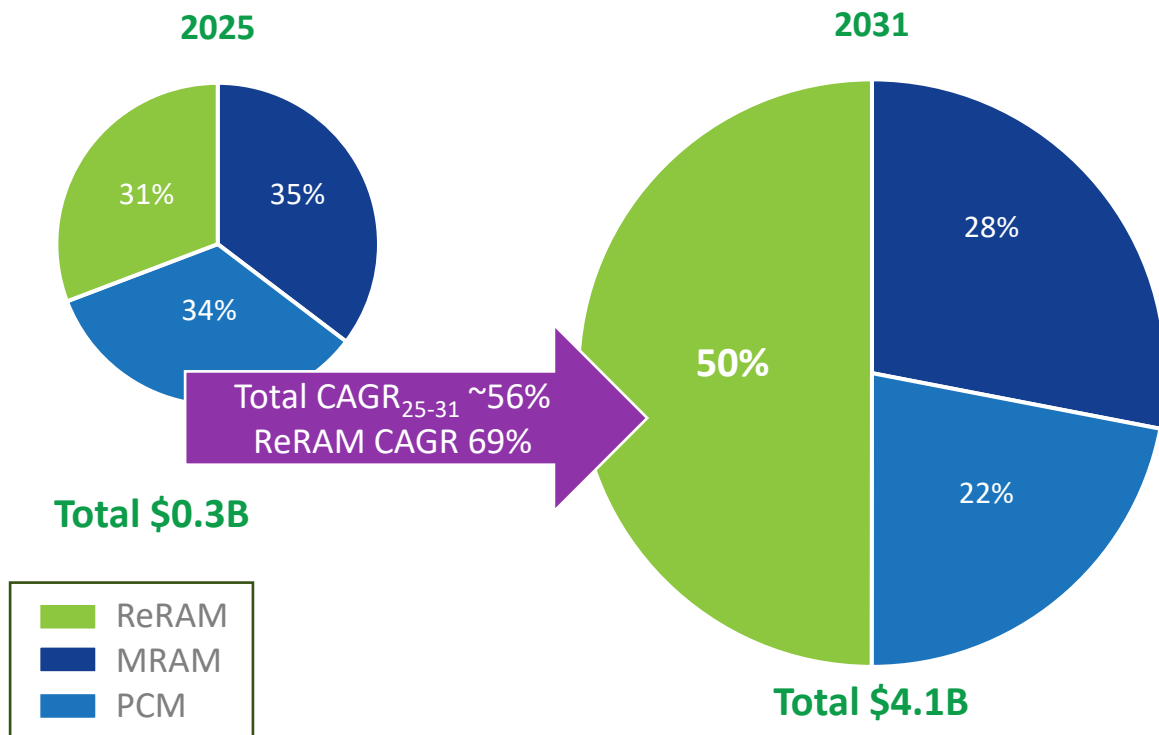
¹ BEOL = Back-End-Of-Line

² Refers to ReRAM cell array

The Rise of ReRAM

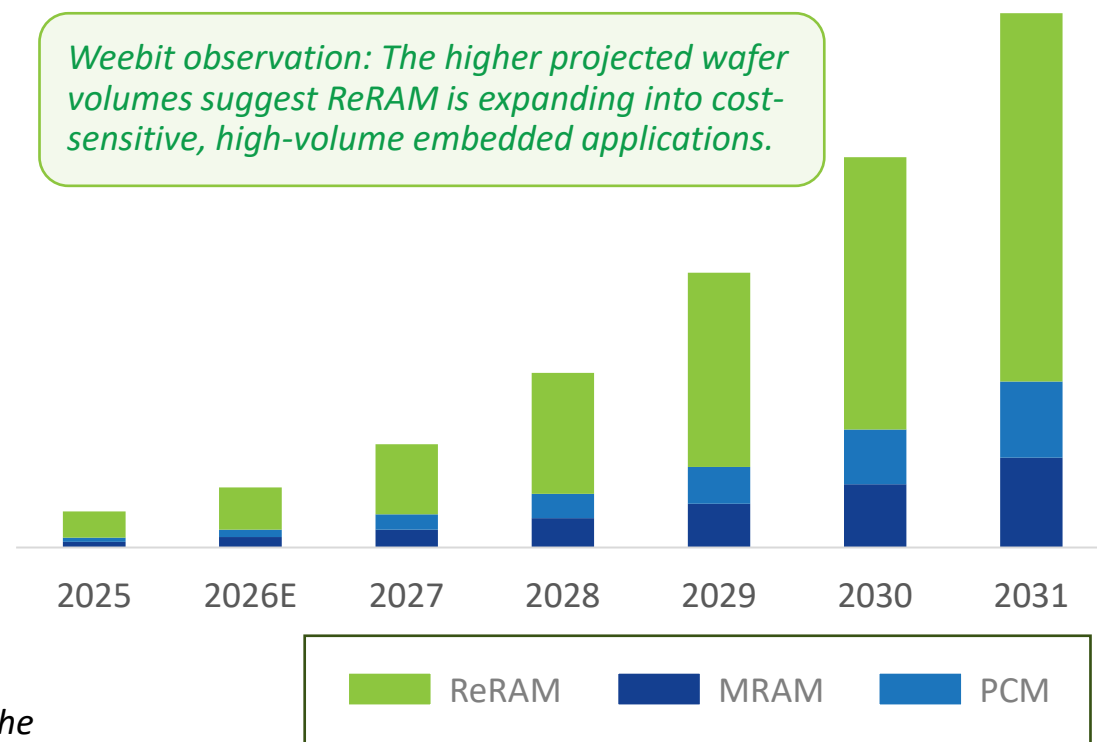
ReRAM outpaces market growth, expanding to 50% share by 2031

Embedded Emerging NVM Market (in \$M)*

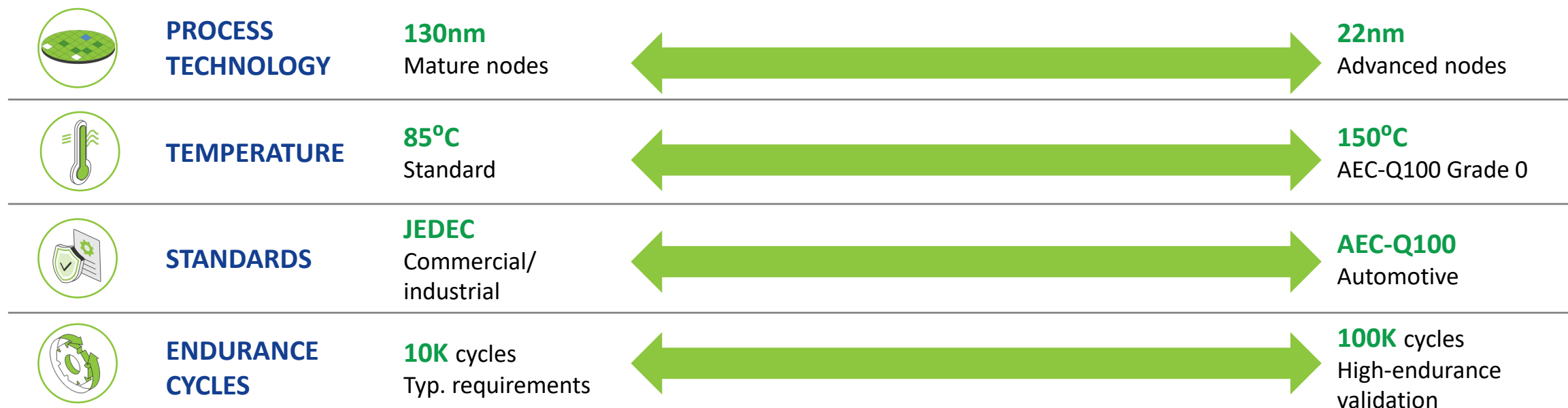


Note: The embedded emerging NVM market size is evaluated based on assumptions of the average chip area occupied by a given memory technology (Yole)

Market Volume in # of Eq. 12" Wafers*



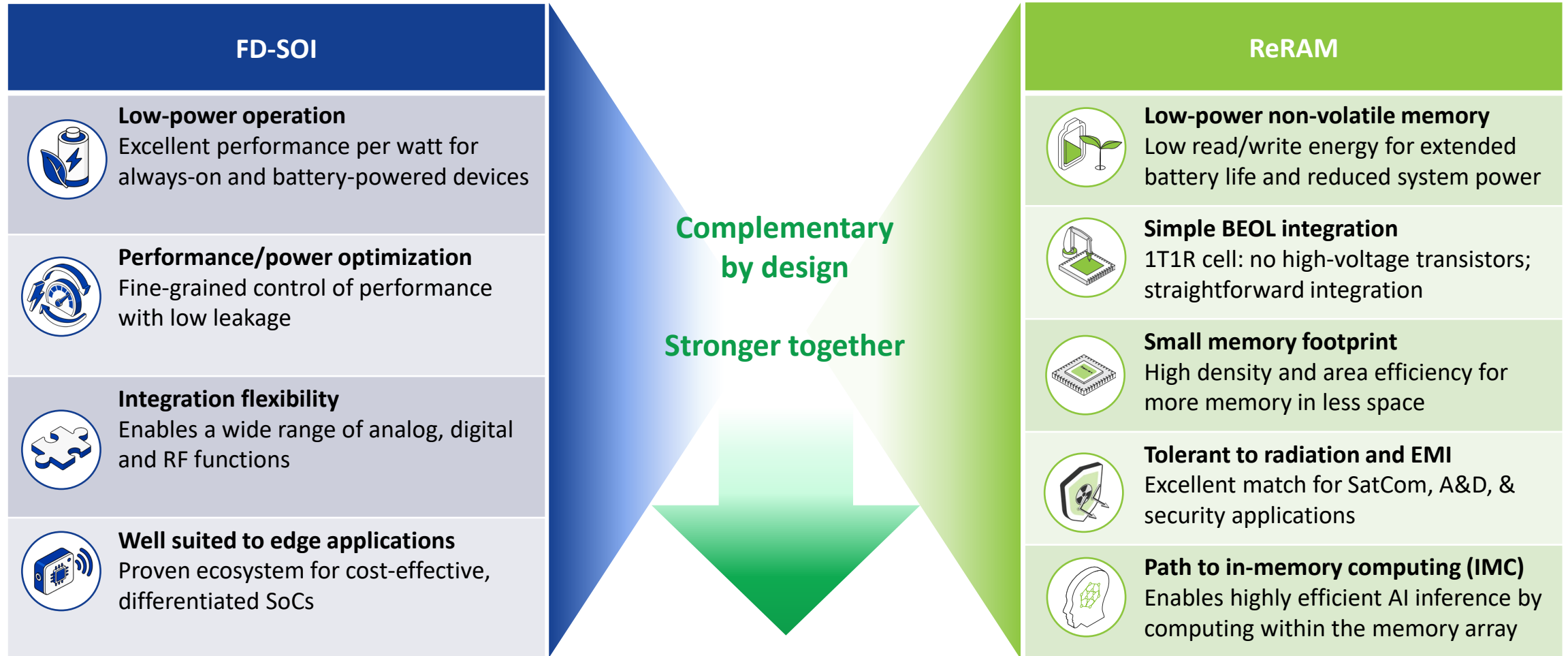
Weebit ReRAM Qualified across a Broad Range of Conditions



SAMPLE QUALIFICATION PROGRAMS

130nm CMOS 125°C; 10K cycles 128/256Kb  JEDEC	130nm CMOS 150/175°C; 100K cycles; 256Kb  AEC-Q100	22nm FDSOI 125°C; 10K cycles 8Mb  JEDEC	65nm BCD 175°C; 100K cycles; xMb  AEC-Q100	130nm CMOS 125C; 10K cycles 1Mb  JEDEC	 Fully Qualified  Qual In Process  Mini-Qual Complete
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ReRAM and FD-SOI: Complementary Technologies for Energy-efficient SoCs

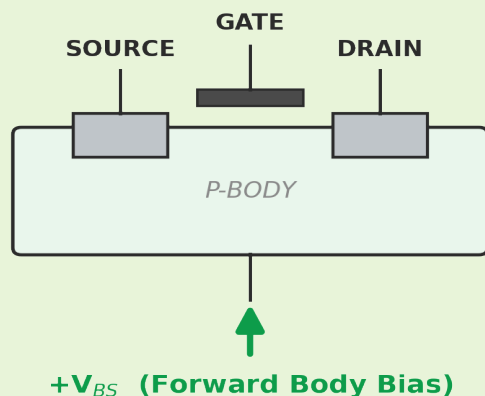


Energy Efficient Edge AI SoCs

ReRAM and FD-SOI: a Perfect Match

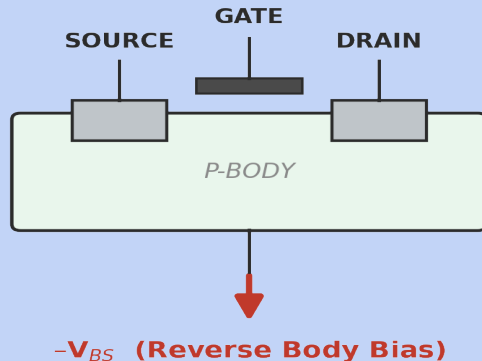
Utilization of Body Biasing

FD-SOI's independent body terminal enables dynamic biasing of ReRAM select devices and periphery circuits without process changes.



Forward Body Biasing (FBB)

Enhances the ReRAM select (1T) programming current transfer capability



Reverse Body Biasing (RBB)

Reduces leakage during programming and read operations



Reliability – Stress Reduction

Reduces stress on select devices and periphery during forming & programming



Analog Corner & Temperature Compensation

Reduces corner & temperature-induced spread in analog circuit performance

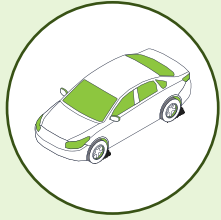
Together, FBB and RBB give ReRAM-on-FD-SOI a flexible way to optimize programming current, leakage, reliability and analog robustness – all from a single body-bias terminal, without altering the process.

ReRAM and FD-SOI: A Broad Applications Landscape

Together enabling low-power, highly integrated SoCs



Cellular



Automotive



IoT



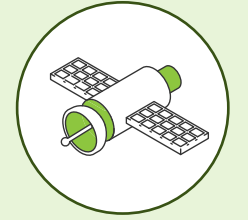
Wearables



Hearing Aids

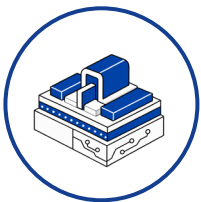


Medical



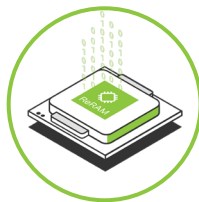
Aerospace &
Defense

One technology combination. Wide application impact.



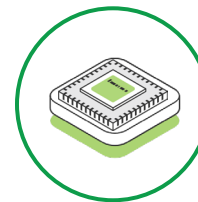
Efficient Process: FDSOI

- Low power, high performance
- Excellent analog/RF integration
- High reliability



Embedded Memory: ReRAM

- Low power; non-volatile
- Fast access; high endurance
- Scalable; simple BEOL integration



Highly integrated SoCs

For a broad range of low-power, high-performance SoCs across mission-critical and intelligent systems

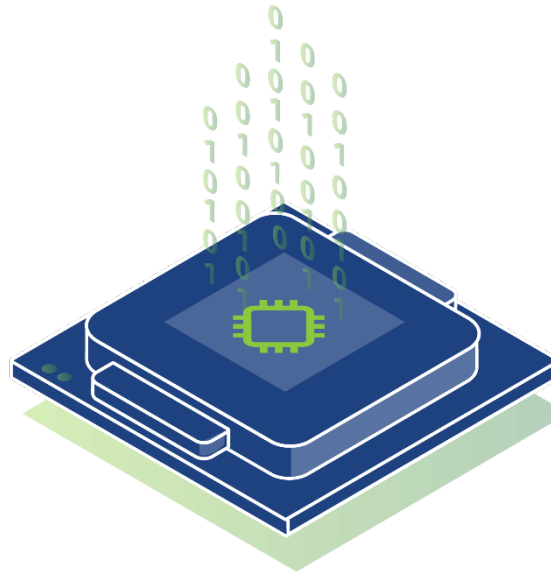
ReRAM for AI Inference

Intelligence is moving to billions of edge devices, creating new demands on memory

More intelligence at the edge

- Larger and more complex AI models
- More parameters, more data, more local storage
- Continuous learning and feature updates

Edge AI devices



Memory challenges increase

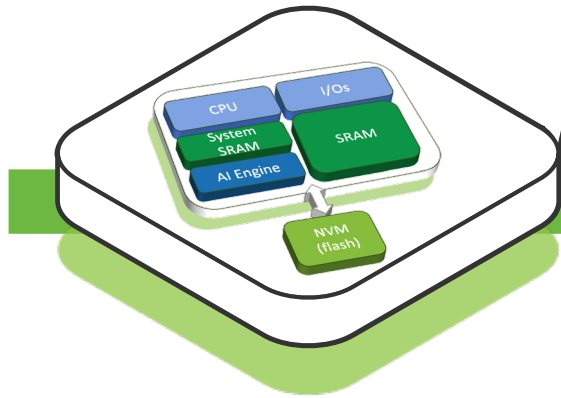
- More on-chip memory capacity required
- High data movement consumes power and adds latency
- Limited energy budget for longer battery life

Real-time inference at low power

ReRAM provides **dense, low-power** non-volatile memory **close to the compute engine**, reducing data movement and enabling efficient, responsive edge AI

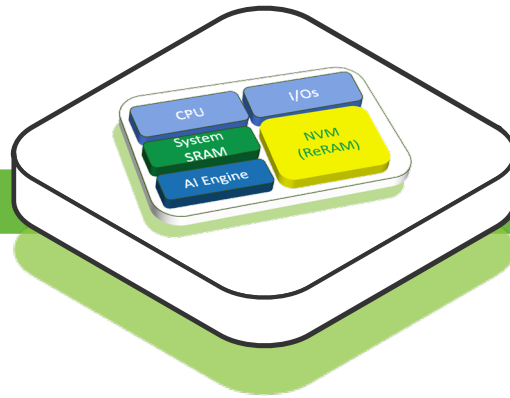
| The Journey to New AI Architectures with ReRAM

TRADITIONAL SOLUTION



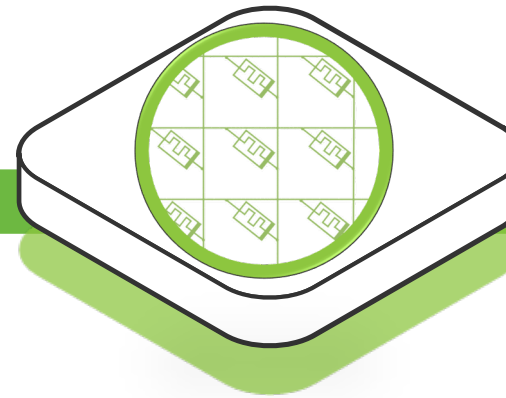
- NVM (flash) on separate chip
- Wasteful in terms of size & cost
 - Prohibitive power
 - Constrained data bandwidth and performance
 - Insecure, vulnerable to hacking

SINGLE CHIP NEAR-MEMORY COMPUTE



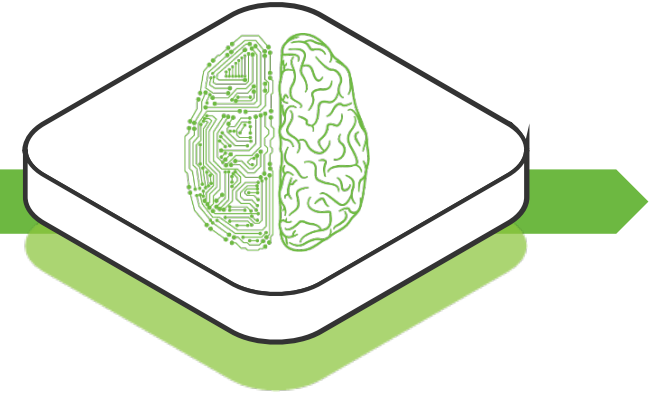
- External NVM eliminated
- Eliminates most data movements → Low-power
 - More efficient storage: **4X greater capacity** than SRAM

IN-MEMORY COMPUTE WITH ReRAM



- Computation performed *within* memory arrays
- **Completely eliminates** data traffic → Ultra-low power
 - Enables **Analog Compute** → Store larger models efficiently

NEUROMORPHIC COMPUTE WITH ReRAM



- Future systems will mimic brain behavior
- Fast real-time processing on **massive amounts of data**
 - Three orders of magnitude **(x1000) better energy efficiency**

ReRAM-based architectures are central to the transformation of AI,
bringing memory and compute together for faster, brain-like intelligence

Why ReRAM for IMC

- ❖ ReRAM allows data storage and matrix-vector computation in the **same physical location**
- ❖ ReRAM can perform multiplication thanks to Ohm's law

$$I_{ij} = G_{ij}v_i$$

Applied
voltage →
input

ReRAM
Conductance
→ weight

Cell Current →
input * weight

- ❖ The crossbar structure can perform the accumulation of all multiplication results, thanks to Kirchhoff's law

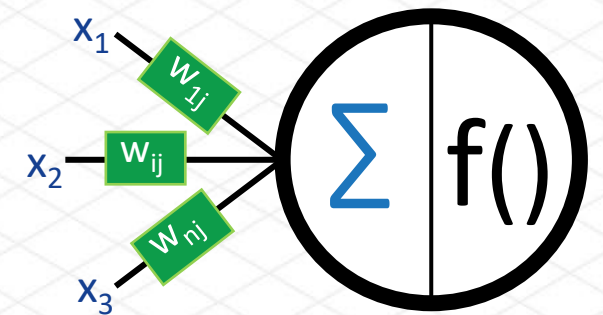
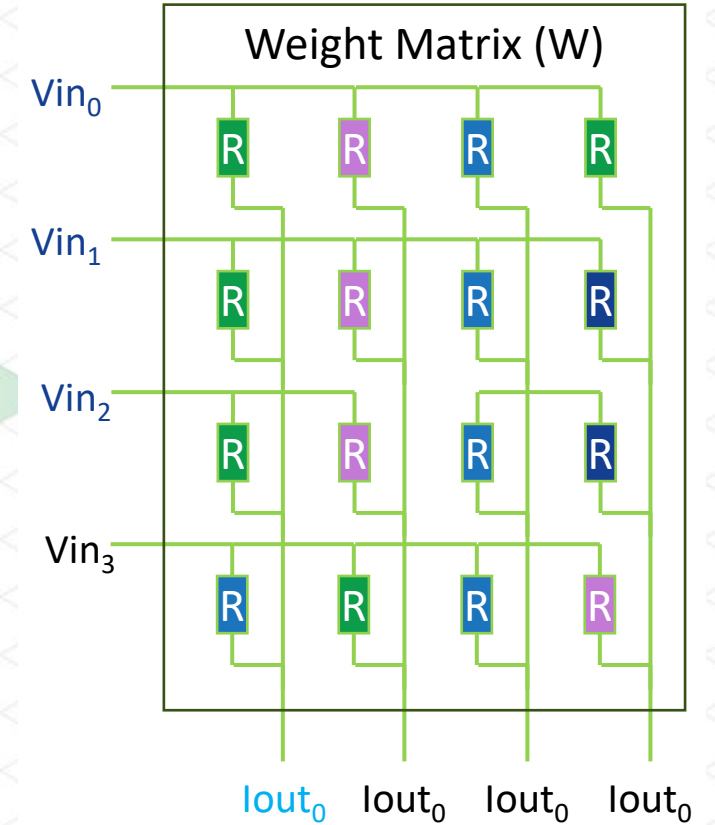
$$I_j = \sum_i I_{ij}$$

Applied
voltages →
input vector

Conductances
→ weight
matrix

Current sum at
the column →
accumulation

- ❖ For IMC, ReRAM offers **very low power, scaling to small geometries, small cell structure, support for MLC**



Weebit ReRAM: A Foundation for Memory + Compute

One technology. Multiple architectures. Broad opportunity.

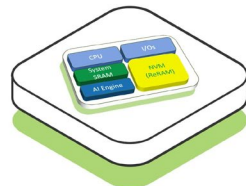
TODAY: Embedded ReRAM

- ❖ Commercially available
- ❖ Qualified on multiple platforms
- ❖ Growing customer adoption
- ❖ Generating revenues

EMERGING: Memory Centric Computing

- ❖ Convergence of memory and compute is transforming AI architectures
- ❖ A growing opportunity for ReRAM

NEAR-MEMORY
COMPUTE



IN-MEMORY
COMPUTE



NEUROMORPHIC
COMPUTE



Why ReRAM?

	Storage	Analog Compute (IMC)	Scalability
Flash	+	+	--
MRAM	+	--	+
ReRAM	+	+	+

💡 The future of AI computing requires memory that is manufacturable, scalable, low-cost, and IMC-ready. Weebit ReRAM is one of the few emerging NVM technologies approaching commercial production.

Takeaways

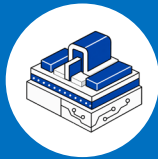
ReRAM + FD-SOI: Enabling the next generation of energy-efficient, intelligent SoCs

Weebit ReRAM is production-ready embedded NVM today



Manufacturable, qualified IP delivering lower power, faster access, high endurance, and small area

ReRAM complements the objectives of FD-SOI



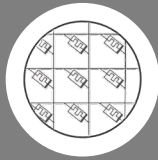
A natural fit for low-power, high-performance, cost-effective and integration-flexible FD-SOI designs

ReRAM addresses the memory requirements of edge AI



Enables more on-chip NVM to support AI inference with low power, high density and minimal data movement

ReRAM provides a path towards in-memory computing (IMC)

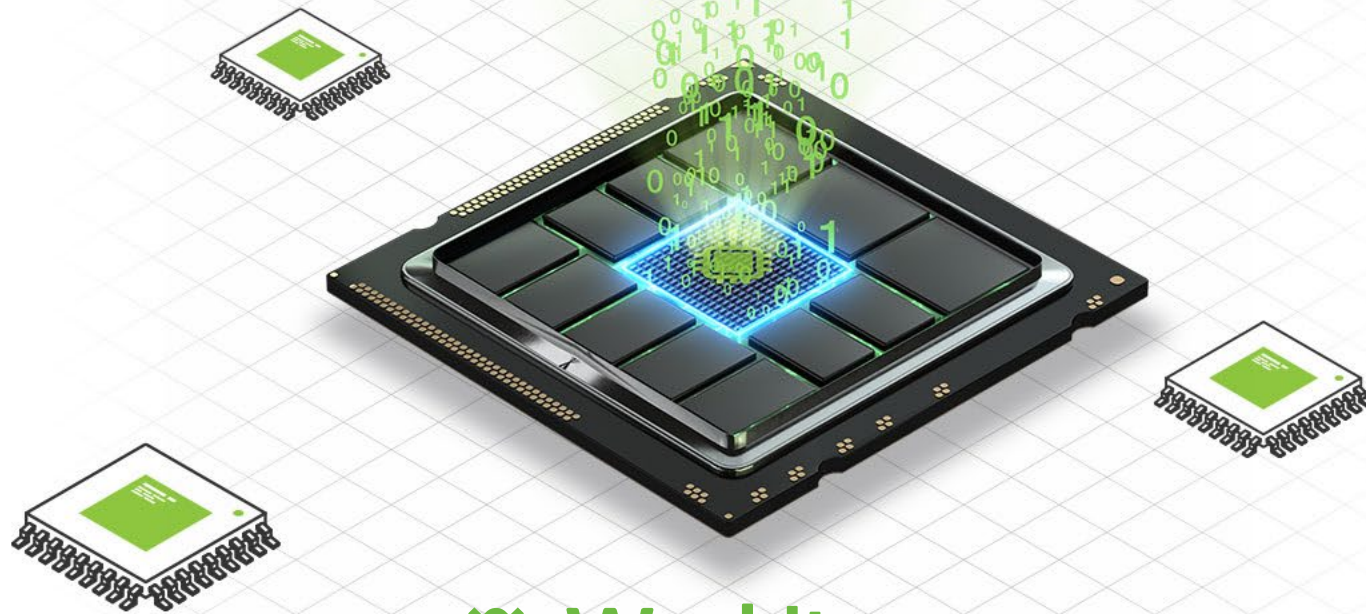


Performance and energy efficiency scale further as computation moves into the memory array

ReRAM bridges today's embedded memory needs with tomorrow's computing architectures – perfectly aligned with FD-SOI

Thank You!

www.weebit-nano.com



 **Weebitnano**
THE NEXT NVM IS HERE