Relaxation-Aware Programming in RRAM: Evaluating and Optimizing Write Termination

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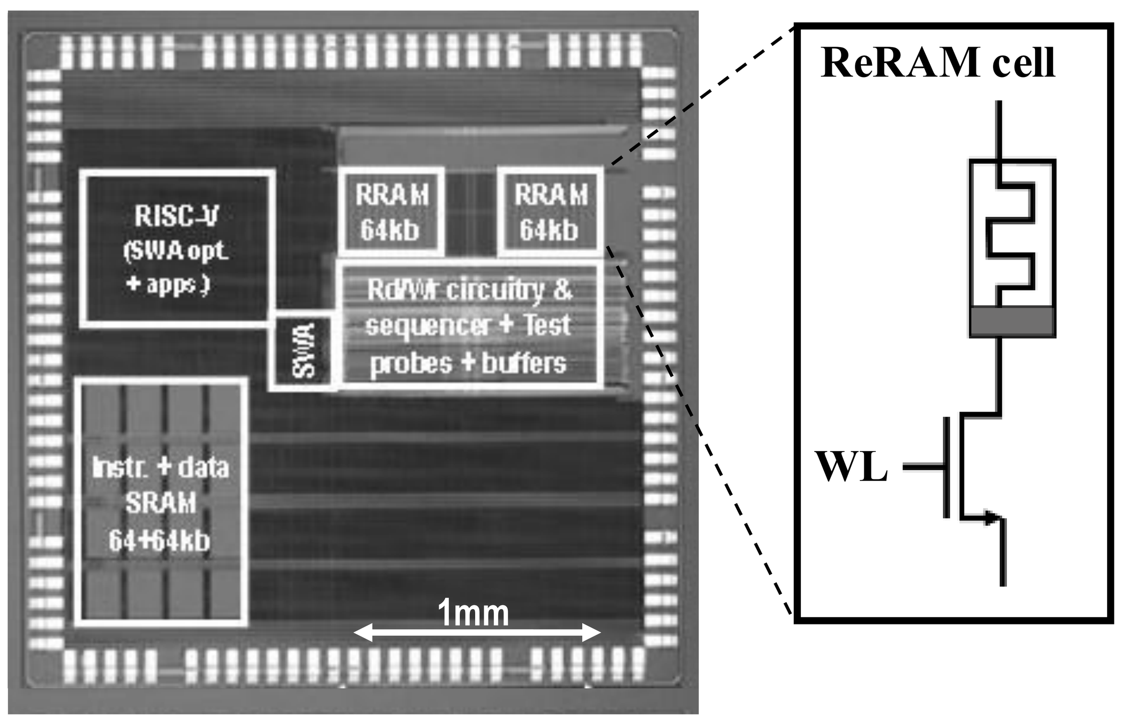
Objectives:
- Improve resistance distribution stability of RRAM arrays
- Assess the impact of write termination (WT) on relaxation of Low Resistance State (LRS)

Proposed Solution:
Increase of SET programming voltage (SET-overdriven WT), leading to:
- Conductance variability reduction, while maintaining WT's power efficiency
- Memory window as wide as constant-duration SET (w/o WT approach)

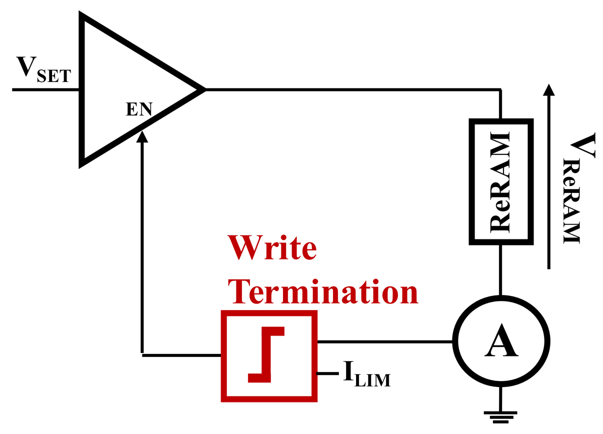
Chip Platform and Write Termination Circuit



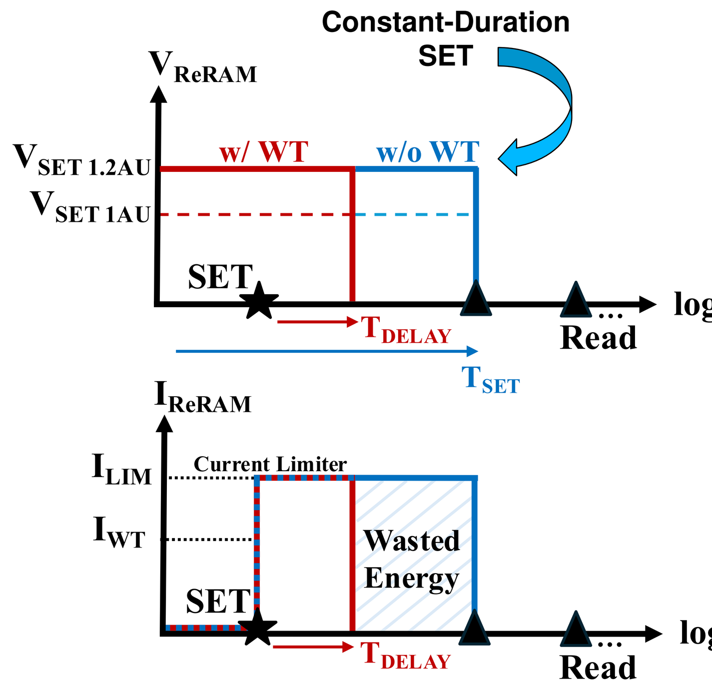
Die photograph and RRAM cell

- The chip embeds a RISC-V subsystem for testing various programming parameters.
- A notable feature of this setup is the configuration of a WT programming.

Technology	130 nm
ReRAM size	128 kb

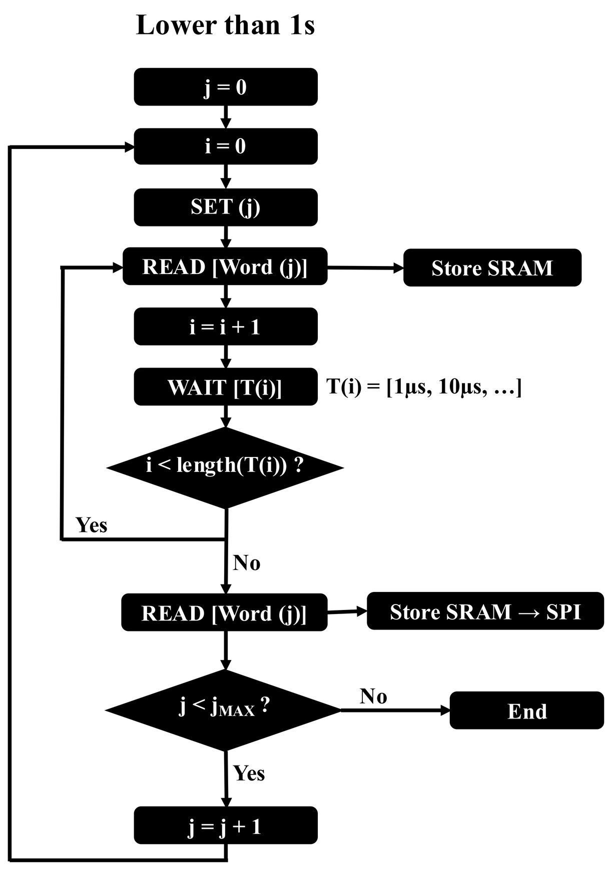


- Halt a write process once the filament formation for SET or disruption for RESET
- Ensure uniform programming energies, enhancing aging
- Improve metrics on access time and energy consumption

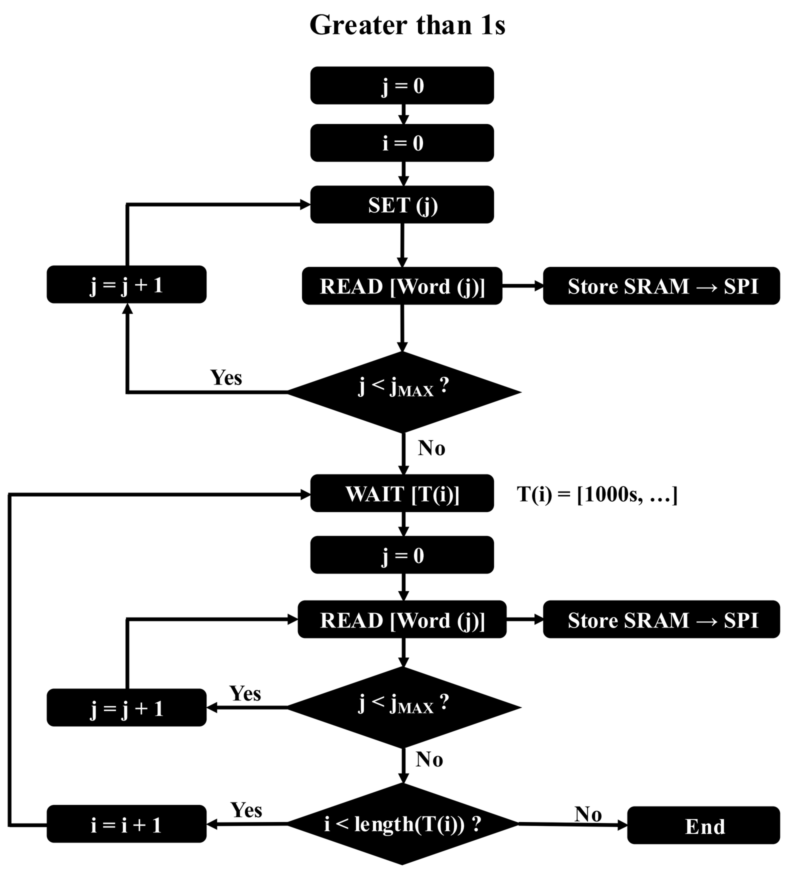


Write Termination Approach

Relaxation Characterization Method and Metrics



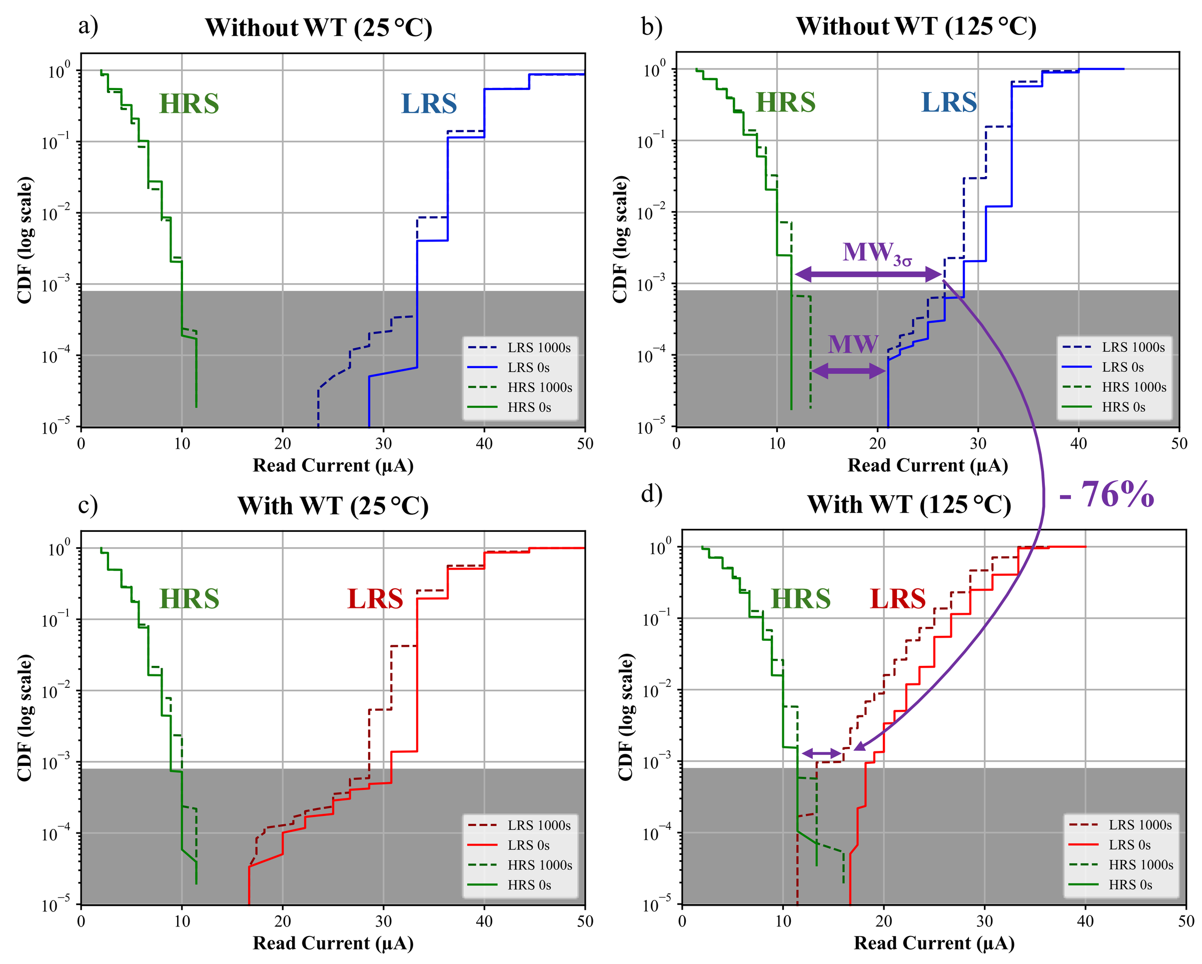
Short time-scale characterization



Long time-scale characterization

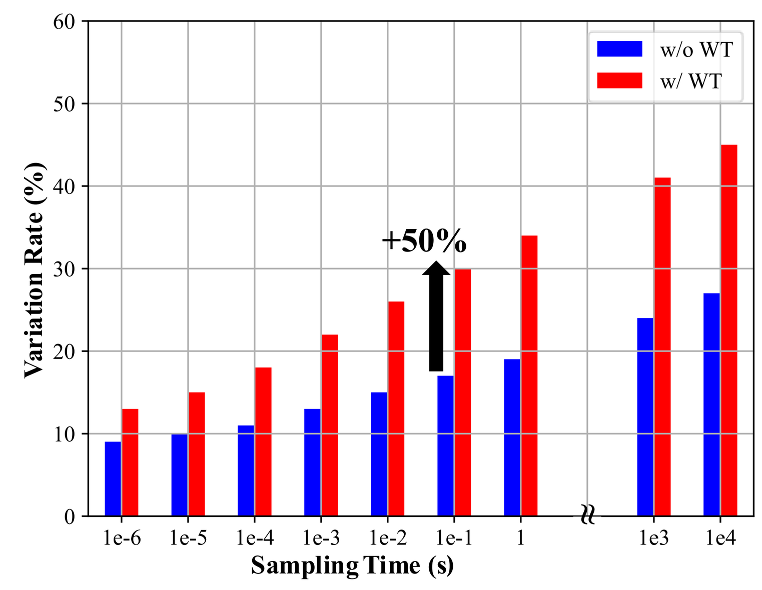
Characterizing Steps for Measuring Relaxation

- Relaxation effects occur across multiple timescales
- Conductance drifts from microseconds to minutes after programming
- Characterization steps:
  - RRAM cells are initialized to the opposite resistance state of the one under evaluation for relaxation effects
  - Program RRAM cells on the resistance state under evaluation
  - RISC-V processor starts a time counter and triggers read operations
  - For shorter time-scale characterization (until 1s):
    - Word-by-word to ensure better precision on read operation timestamps
  - For longer time-scale characterization (from 1s to 10^4s):
    - The entire RRAM macro is fully programmed and then fully read.



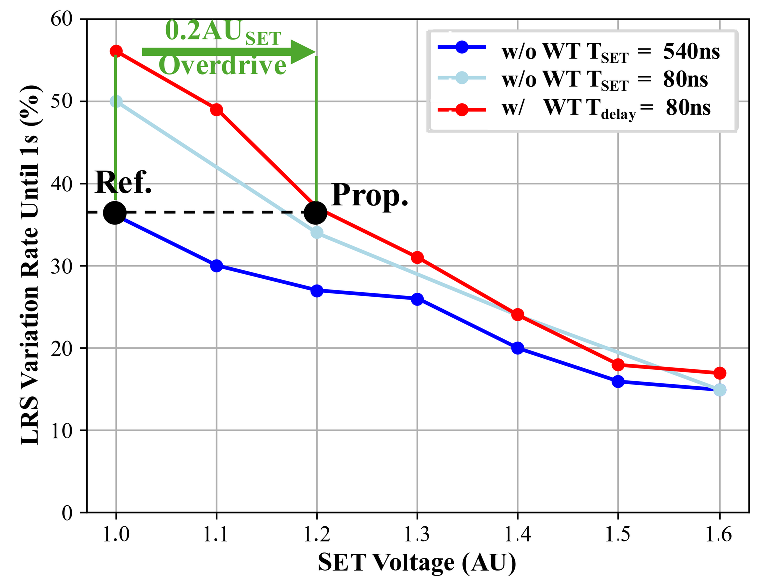
CDFs of Read Current Distributions w/ and w/o WT

Temperature influences results w/ and w/o WT. Relaxation shift is more pronounced when WT is enabled.

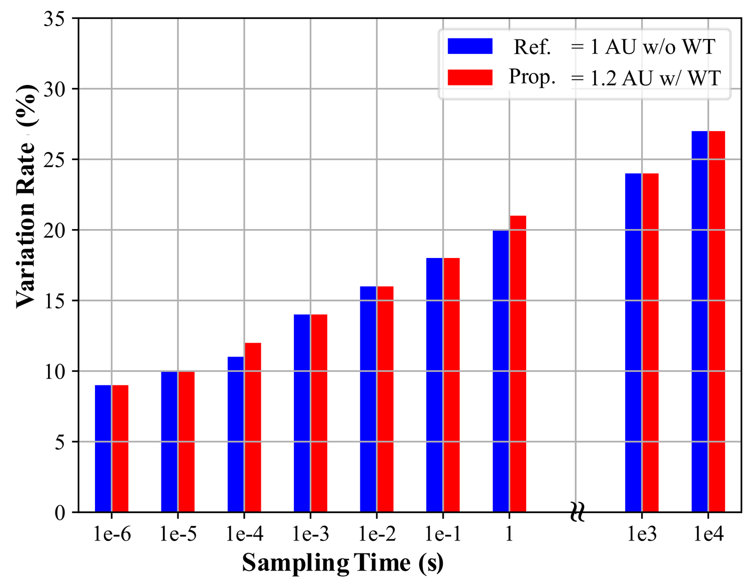


Evolution of Variation Rate at 25°C

- **Variation Rate** is the fraction of cells that exhibit a change in conductance relative to their initial programmed value
- Enabling WT leads to a significantly higher variation rate (+50%), and this ratio remains relatively stable over time.



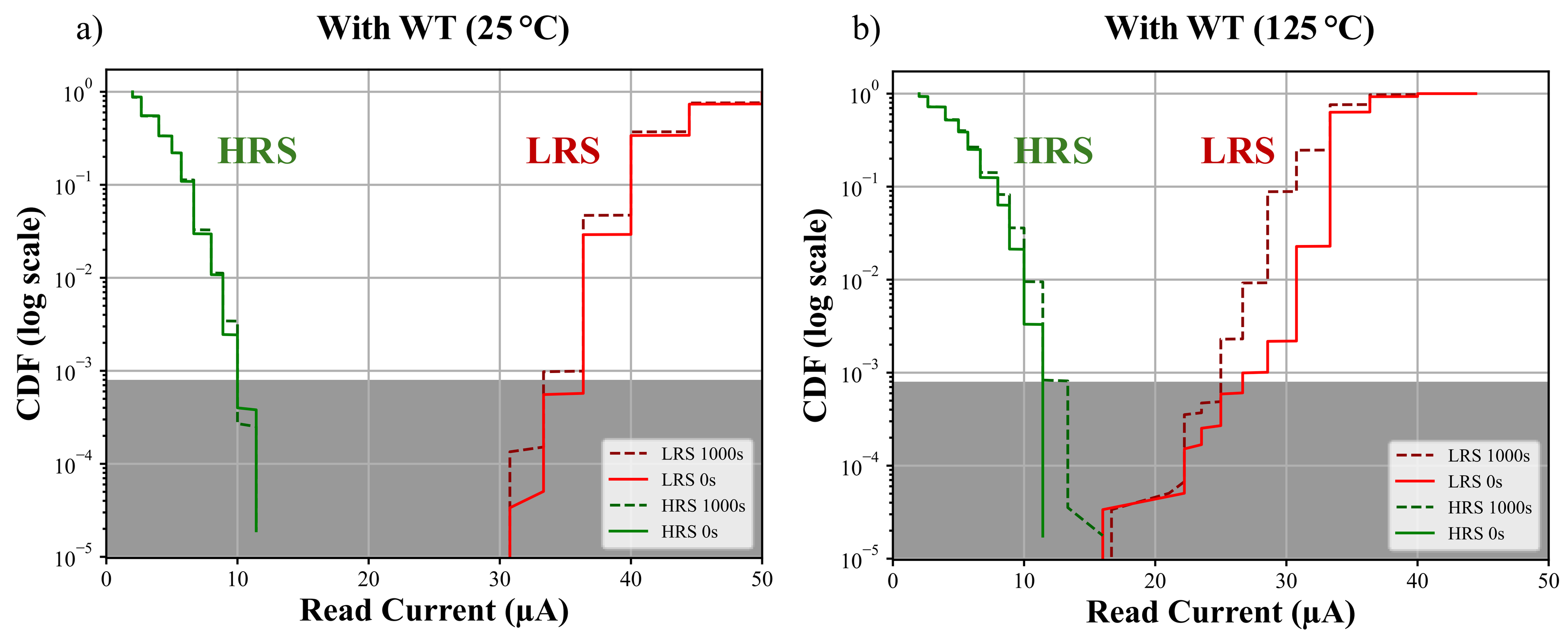
SET Voltage Overdrive



Evolution of Variation Rate after SET Voltage Overdrive at 25°C

- SET voltage significantly influences the variation rate.
- Higher voltage reduces conductance drift even with WT.

Enhanced CDFs with SET Voltage Overdrive



CDFs of Read Current Distributions After SET Voltage Overdrive

Higher temperatures exacerbate relaxation effects, but overdriven SET successfully limits conductance drift to levels comparable to constant-duration SET.

Conclusion

Summary of Set Techniques with WT

	V_{SET} (AU)	1		1.2	
	Time (s)	0	1000	0	1000
MW at 3σ	25°C	-15%	-31%	-26%	-26%
	125°C	-41%	-76%	0%	0%
MW w/ tail bits	25°C	-48%	-39%	+5%	+22%
	125°C	-100%	-100%	-38%	-45%
Energy Consumption		-56%		-47%	
Time for 50% Variation Rate		< 1 Day		>> 10 Years	

* Constan-duration SET used as reference.
** Energy consumption is estimated from [1]

The overdriven SET technique:
- Effectively reduces conductance drift
- Preserves the energy-saving benefits of WT
- Achieves a memory window comparable to constant-duration SET
- Viable solution for energy-efficient, relaxation-aware programming.

[1] B. Giraud et al., "Smart Write Algorithm to Enhance Performances and Reliability of an RRAM Macro," IEEE J. Solid-State Circuits, vol. 59, no. 9, pp. 3045–3057, Sep. 2024