ReRAM: From Concept to Product

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NVMTS 2022 select, redacted slides
Agenda

- Weebit Nano introduction
- ReRAM basic operation
- Lab-to-market challenges – Road towards product qualification
- Conclusions
Who We Are?

Leading developer of innovative next-generation memory technologies for the global semiconductor industry

We are enabling a leap forward in memory technology for a new era of connected devices

**Founded: 2015**
Located in Israel & France
ASX: WBT

**World-leading team**
50 personnel* (90% engineers/ scientists)

**R&D partner**
CEA-Leti, leading micro-electronics research institute

**Financial strength**
Raised A$35m in Nov. 2021 Well funded to 2024

**Current business model**
Product & IP licensing to semiconductor companies & fabs

**Process nodes**
130nm, 28nm, 22nm under development
Bulk, FD-SOI, FinFET

**Signed 1st commercial deal**
Ongoing discussions with additional fabs and customers

**Technology status**
1st memory module demonstration; Successfully qualified IP module

**Silicon-proven technology**
Volume production expected 2023
Proven in production-fab wafers

*Includes employees and full-time contractors
Weebit-Leti Development Partnership

- Weebit is collaborating with CEA-Leti since 2016 to develop its ReRAM
  - Leveraging >10 years of ReRAM research at Leti
  - Weebit has full rights to all ReRAM-related IP
- The Weebit-Leti development collaboration is yielding exciting results:
  - Mbit arrays demonstrated at 28nm – 130nm
Cost Effective ReRAM NVM

- **2-mask adder**
  - Very few added steps

- **Fab-friendly materials**
  - No contamination risk, special handling, etc.

- **Using existing deposition techniques and tools**
  - Easy to integrate into any CMOS fab

- **BEOL technology**
  - Stack between any 2 metal layers
  - No interference with FEOL
  - Easy to scale from one process variation to another
ReRAM Basic Operation

- **SET (Program)** – HRS -> LRS
- **RESET (Erase)** – LRS -> HRS
# ReRAM Fits Various App Requirements

<table>
<thead>
<tr>
<th>Feature</th>
<th>Mixed-Signal / Power Mgmt</th>
<th>IoT / MCUs</th>
<th>Edge AI</th>
<th>Automotive</th>
<th>Aerospace &amp; Defense</th>
</tr>
</thead>
<tbody>
<tr>
<td>Back-end-of-line tech for easy analog integration</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Cost-efficiency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
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<tr>
<td>Ultra-low power consumption</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
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<tr>
<td>Robustness in high temp / extreme environments</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Scaling advantage at 28nm and below</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Endurance</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Small footprint to store very large arrays</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Longevity</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
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</tr>
<tr>
<td>Roadmap to neuromorphic computing</td>
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<td></td>
<td>✓</td>
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</tbody>
</table>
Making a Memory Product
Technology Demonstrations

SPIRIT Demo in **FMS 2019**

1st ever analog spiking neurons and ReRAM based synapses

Module Demo in **LID 2022**

Embedded ReRAM with RISCV processor
Weebit ReRAM Module Design in Qualification

- Integrating a ReRAM array in a complete module in 130nm technology
- The module includes:
  - All analog circuitry
  - Smart algorithms (read, set/reset, forming)
  - Control logic and data manipulation
  - Redundancy, ECC
- The ReRAM module is further integrated into a complete subsystem based on a RISC-V processor
- Qualification concluded successfully

Module design is tightly coupled with Weebit’s process & memory cell
The Road from Design to Market
Technology Concept

- Every new technology starts with a concept
- Finding a promising materials set that demonstrates superior memory operation
- Performance should be groundbreaking – Advantages against the state-of-the-art
- Manufacturability – Not every material is fab-friendly or easy to integrate / process
- Cost effective solution – Should not include many added layers, special tooling or complicated process

Technology needs to be simple & easy to integrate
It's All About Statistics

Each new technology starts with few single cells, BUT:

- How will they behave if we put a million of them together on the same chip?
  - What does their distribution look like?
  - How is their cell-to-cell variability? Does the distribution have tails?
  - Does the farthest cell get the same condition as the nearest cell?

- If we put millions of them on the same chip, how will they behave across an entire wafer?
  - What is their die-to-die variability? Is performance uniform?
  - What is the die yield (number of good dies per wafer)?

- What is the variance between different wafers and different production lots?
  - Does each lot have different results?
  - What is the lot-to-lot variability?
  - Is there any sensitivity to process variations?
In bit cell technology development, we look at analog value distributions.

Now we treat the values as data of zeros and ones, not just resistance values.

For a product to work, it needs to have no errors, otherwise data will be corrupted, or code will not execute correctly.
Product Characterization & Qualification

❖ Characterization
   ◆ Many conditions must be tested to determine performance to cover all operating conditions
     • Testing functionality at three temperatures – Cold (-40°C), Room and Hot (85 °C/125 °C/150 °C)
     • Testing at spec voltage range (Min, Type, Max)
     • Testing corner lot to create process variations (Fast, Typical, Slow)

❖ Qualification
   ◆ Testing three production lots samples at different times for the following:
     • Endurance
     • Retention
     • Read Disturb

Characterization & qualification can take some time
### NVM Qualification Requirements

Hundres of dies, blindly selected from 3 independent production lots, must pass 100% of tests defined by JEDEC:

<table>
<thead>
<tr>
<th>Stress</th>
<th>Test Item</th>
<th>Reference</th>
<th>Stress Conditions</th>
<th>Test Conditions / Acceptance Criteria</th>
<th>Sample Size</th>
<th>Comments</th>
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</thead>
<tbody>
<tr>
<td>NVCE</td>
<td>Endurance</td>
<td>JESD22-A117</td>
<td>Room and Hot</td>
<td>Datasheet Spec/ 0 Fails</td>
<td>3 Lots/ 77 units</td>
<td>Test all the array bits</td>
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<tr>
<td></td>
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<td>JEDEC 47</td>
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<tr>
<td>UCHTDR</td>
<td>Data Retention</td>
<td>JESD22-A117</td>
<td>Tstress – 125°C</td>
<td>1000 hrs/ 0 Fail</td>
<td>3 Lots/ 77 units</td>
<td>Readout at room and hot</td>
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<tr>
<td></td>
<td></td>
<td>JEDEC47</td>
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</tr>
<tr>
<td>PCHTDR</td>
<td>Post Cycle Data Retention</td>
<td>JESD22-A117</td>
<td>Tstress = 125°C 100% spec</td>
<td>10 hrs/ 0 Fail</td>
<td>3 Lots/ 39 units</td>
<td>Readout at room and hot</td>
</tr>
<tr>
<td>SMT</td>
<td>SMT Reflow</td>
<td>ESD22-A113</td>
<td>Tc 260 °C</td>
<td>3 cycles/ 0 fails</td>
<td>3 Lots/ 25 units</td>
<td>Pb-Free Assembly Profile</td>
</tr>
</tbody>
</table>

All Weebit ReRAM units passed all tests with zero failures
Non-Volatile Cycling Endurance (NVCE)

- Repetition of high stress during programming can lead to dielectric degradation due to defect generation
- After too many cycles, the dielectric can break leading to stuck LRS
- By smart algorithm we can reduce the stress and not break the filament

*D. Alfaro Robayo, IEEE TED 2019*
Non-Volatile Cycling Endurance (NVCE)

- For Program/Erase Endurance Cycling, a data change occurs when a stored “1” is changed to a “0”, or when a stored “0” is changed to a “1”
- Failure occurs when a write or erase data pattern within the memory array does not correspond to the intended data pattern

```
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
000000000000000
000000000000000
000000000000000
000000000000000
000000000000000
000000000000000
000000000000000
000000000000000
000000000000000
000000000000000
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
111111111111111
```

X10K Times
Data Retention

- Data retention is a measure of the ability of a memory cell in an NVM array to retain its charge state in the absence of applied external bias.
- Data retention failure occurs when a memory cell no longer detected to be in its intended data state.
- A bit flip is defined as the failure of a bit to retain its data state after a program or erase operation.

BEFORE STRESS

AFTER STRESS
Conclusions

- After several years of development, Weebit demonstrate a qualified technology at 130nm with good demonstration at 28nm

- Excellent data retention and endurance is demonstrated on our first embedded IP Module demo chip

- 1st module with Leti is fully qualified at hot temp while our 2nd module at SkyWater is now starting qualification
Thank You!

www.weebit-nano.com