PITT STREET RESEARCH

Weebit Nano Ltd.

Scaling down ReRAM to 22nm

Weebit Nano (ASX:WBT) announced it is working together with development partner Leti to scale down its Resistive Random Access Memory (ReRAM) technology for embedded applications to 22 nanometers (nm). Specifically, the company is targeting the so-called Fully Depleted Silicon-On-Insulator (FDSOI) process at 22 nm. Previously, WBT had already successfully demonstrated its technology at the 28nm, 40nm and 130nm nodes. Once completed, this further scaling of its technology to a smaller geometry for FDSOI will enable WBT to address the fast-growing market for low-power embedded devices.

Why scaling down to 22 nanometer is so important

Chip manufacturers are always looking to improve their products in the areas of performance, power consumption and manufacturing costs. Making chips smaller by shrinking the various elements helps in all these areas and 22nm is currently a major process node in the semiconductor industry.

What is fully-depleted silicon-on-insulator?

FDSOI is a semiconductor technology that delivers the benefits of smaller resolutions mentioned above, but uses a simplified manufacturing process with fewer process steps and fewer masks involved. A number of semiconductor manufacturers have been using FDSOI at various nodes for a number of years already. Therefore, we believe ReRAM embedded in FDSOI at 22nm will be a winning combination for WBT.

To boldly go where other NVM's can't

FDSOI is used in low-power devices, most notably Edge devices, including applications such as 5G, Automotive and Artificial Intelligence. These devices are getting smaller every year, which places increasingly stringent requirements on the semiconductors used. One of the main bottlenecks in scaling down the overall chip is the embedded memory component in these devices, which currently mostly comprises SRAM and NAND Flash memory. However, SRAM is volatile and not as efficient as ReRAM, and Flash memory doesn't scale down below 40nm. This is where ReRAM comes in. If and when WBT succeeds in scaling down its technology to 22nm, we believe there is a substantial market waiting to be conquered.

Valuation of A$4.75 per share

We reiterate our valuation for WBT of A$4.75 per share (see full valuation *here*). Additionally, we believe the recent share price development of industry peer BrainChip (ASX:BRN), which was briefly worth A$4BN in January 2022, indicates the potential for ASX-listed semiconductor companies that can successfully commercialise. Even at its current valuation of A$1.8BN, BRN's valuation is ~4x higher than WBT's.

Share Price: A$2.71

ASX: WBT

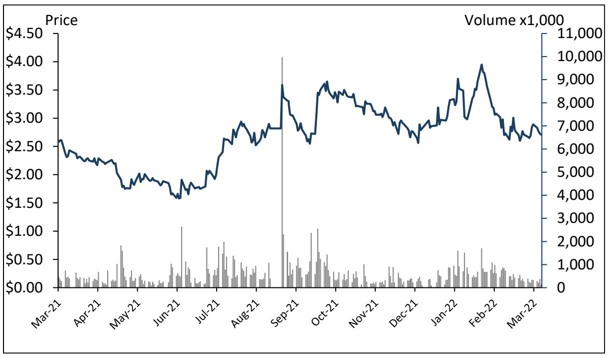
Sector: Technology Hardware & Equipment

25 March 2022

Market Cap. (A$ m)	466.2
# shares outstanding (m)	172.0
# share fully diluted	189.0
Market Cap Ful. Dil. (A$ m)	512.3
Free Float	100%
52-week high/low (A$)	$4.48 / $1.55
Average daily volume (x1,000)	611
Website	www.weebit-nano.com

Source: Company, Pitt Street Research

SHARE PRICE (A$) AND AVG. DAILY VOLUME (K, R.H.S.)



Source: Refinitiv, Pitt Street Research

Valuation metrics	
Valuation per share (A$)	4.75

Source: Pitt Street Research

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Disclosure: Pitt Street Research directors own shares in Weebit Nano Ltd.

Please see page 5 for an overview of key investment risks.

Table of Contents

22nm resolution opens up many opportunities

Moore's Law, named after one of the founders of Intel (NASDAQ:INTC), originally stated that the number of transistors on a computer chip would roughly double every 12 months. Later on, Moore revised his "law", which is actually more of an observation/prediction, to a doubling of the number of transistors roughly every 24 months. While this law has held up for a long time, in the last 10 years it has become exponentially harder and more expensive for the semiconductor industry to keep up this doubling of transistors every two years due to technological challenges. At the so-called leading edge of chip manufacturing, i.e. the most advanced chips, the industry is currently working to get down from 5nm to 3nm and then 2nm.

22nm is one of the main production nodes today

However, that is the leading edge, only applicable to the most advanced and expensive applications, like semiconductors for high-end mobile phones, 5G equipment etc. Most commercial chip production is done at less challenging resolutions, i.e. higher than 20nm. This is where the commercial opportunity for WBT is, in our view. Which is why scaling down from the 28nm node to the 22nm node is so important as it will present WBT with many additional commercial opportunities with potential customers that need non-volatile memory solutions at 22nm rather than 28nm, potentially in increasingly large volumes.

NAND Flash memory can't scale below 40nm

NAND Flash memory can be used as both embedded and stand-alone memory, the latter being the largest global application area for Flash currently. WBT is developing and optimising its ReRAM technology to work in both application areas.

Cross-talk prevents NAND Flash memory to be scaled down lower than 40nm

As we have spoken about in previous research reports on WBT available here, NAND Flash memory doesn't scale below 40nm in a cost-effective way. Below 40nm, Flash memory cells start to experience cross-talk, i.e. leakage of currents to adjacent cells. Solving that problem at smaller resolutions would make Flash memory too costly. That's why Flash memory manufacturers started to build 3D NAND Flash memory for stand-alone memory, i.e. stacking memory cells on top of each other, like apartments in a skyscraper. With ReRAM, that's not necessary as it scales down to much smaller linewidths in a cost effective way.

ReRAM is also faster and uses substantially less power than Flash memory

On top of that, 3D NAND Flash only works for stand-alone memory and is not a solution for embedded memory. So, in small geometries that require NAND Flash, a chip manufacturer will need to use external memory, which is slower and consumes more power.

Flash memory uses substantially more power than ReRAM, which means the latter is much more suited to low-power Edge applications where battery life is a big concern. ReRAM switching speeds are also substantially faster than Flash.

Overall, we believe ReRAM at 22nm will provide WBT with many commercial opportunities going forward.

Fully-depleted silicon-on-insulator

In their efforts to improve performance, power consumption and manufacturing costs of non-volatile memory, chip manufacturers are always looking for more efficient and relatively (cost per chip) cheaper production methods.

Fully-depleted silicon-on-insulator (FDSOI) is an innovative semiconductor technology that delivers the benefits of smaller resolutions and uses a simplified manufacturing process with fewer process steps and fewer masks involved.

Fully depleted means the transistor hasn't been doped

One of the innovations used in FDSOI is the use of an ultra-thin layer of insulator on top of the wafer, so-called buried oxide. A very thin silicon film is then deposited to form the transistor channel. Because it's so thin, the electrical, optical and structural properties of the transistor channel are already so good that it doesn't need to be doped, which lowers the number of process steps and thus production costs, although SOI wafers in general are typically more expensive than CMOS wafers. Doping refers to the introductions of small amounts of impurities to the transistor to improve the electrical characteristics in particular. In the absence of doping, the transistor is *Fully Depleted.*

Lower current leakage required to scale down further

One of the main benefits of FDSOI, apart from a simpler manufacturing process, is substantially lower current leakage, which is important as the industry scales down from the current *workhorse* node of 28nm to 22nm and 20nm. A number of semiconductor manufacturers, including Samsung, TSMC, GlobalFoundries and IBM, have been using FDSOI at various nodes for a number of years already. Therefore, we believe ReRAM embedded in FDSOI at 22nm (and maybe 20nm) will be a winning combination for WBT.

Valuation for WBT of A$4.75 per share

Fair value of A$4.75 per share reiterated

In our research update on WBT from January 2021, available here, we valued the company at A$4.75 per share using semiconductor industry M&A transactions and parallels to ASX-listed peer BrainChip (ASX:BRN).

Following the commercial agreement with SkyWater and the company's most recent announcement regarding scaling down to 22nm, we reiterate our A$4.75 per share valuation.

Industry peer BrainChip gives insight into WBT's potential upside

WBT's closest ASX-listed peer when it comes to commercialisation, BrainChip (ASX:BRN), has seen a strong uplift in valuation recently, helped by a new commercial agreement it signed late in 2021 with MegaChips in Japan. Additionally, an announcement by Mercedes regarding the use of BRN's Akida in a concept car drove the share price to new highs.

BrainChip (ASX:BRN) was briefly valued close to A$4bn

BRN was briefly valued at close to A$4BN before the share price retreated to the current level. At the current share price, the market values BRN at approximately A$1.8BN, i.e. approximately 4x WBT's current market cap. In our view, BRN's share price movements over the last few months signal the potential for WBT if it can demonstrate successful qualification with SkyWater and ongoing commercialisation with additional new customers.

Key investment risks

- Although WBT is getting closer to commercialisation, the company has yet to qualify the technology in SkyWater's manufacturing facilities, which involves execution risk. Hence, there is a risk that the potential of WBT's technology may be delayed or may not eventuate.
- Alternative emerging memory technologies are being developed by WBT's competitors. These technologies could potentially be superior in

nature and/or could be commercialised sooner than WBT's technology, which would inhibit the company's future growth.

However, apart from 4DS Memory (ASX:4DS), we don't see the other ReRAM players, specifically Crossbar and Adesto, as potential competitors. Crossbar seems to have "evaporated" with no significant business activity in the last 18 months, while Adesto was acquired by Dialog Semiconductor for an EV of US$500m (A$758m at the time), specifically for its IP in the IoT space. Dialog was subsequentially acquired by Renesas (2021).

- Although WBT now seems adequately funded for the medium term, the company may need to raise further capital. That may be required, for instance, if its current development programs and technology transfer/qualification take longer than currently anticipated or multiple growth opportunities arise, resulting in dilution for existing shareholders (albeit at offer prices reflecting the company's progress).
- COVID-19 still poses a potential risk to WBT as potential inability to travel may pose challenges to WBT's technical and commercial people in its conversation with partners and prospects. This may slow down further commercialisation.

Please refer to www.pittstreetresearch.com for our initiating coverage report on WBT, including more elaborate risk assessments.

Appendix I – ReRAM technology

ReRAM technology: The right balance between Flash memory and DRAM

ReRAM is a fast, cost-effective and energy-efficient NVM technology. It can be considered a hybrid memory technology, as it is non-volatile like Flash memory and nearly as fast as DRAM, which is volatile, i.e., a DRAM cell will lose the value (1 or 0) that is stored if the power is switched off. WBT is developing SiOx ReRAM, which, in terms of performance metrics, sits right between Flash and DRAM.

How does it work?

Generally, in case of NAND Flash memory, the values of 1 and 0 are attributed on the basis of the trapped electrical charge present in the memory cell's floating gate. However, in case of a ReRAM cell, the values (1 and 0) are attributed based on the resistance level of the cell material sandwiched between the two electrodes (Figure 1). A value of 1 is attributed to a state of low resistivity, while a value of 0 is attributed to a state of high resistivity.

There are two ways of changing the resistance level of a ReRAM cell.

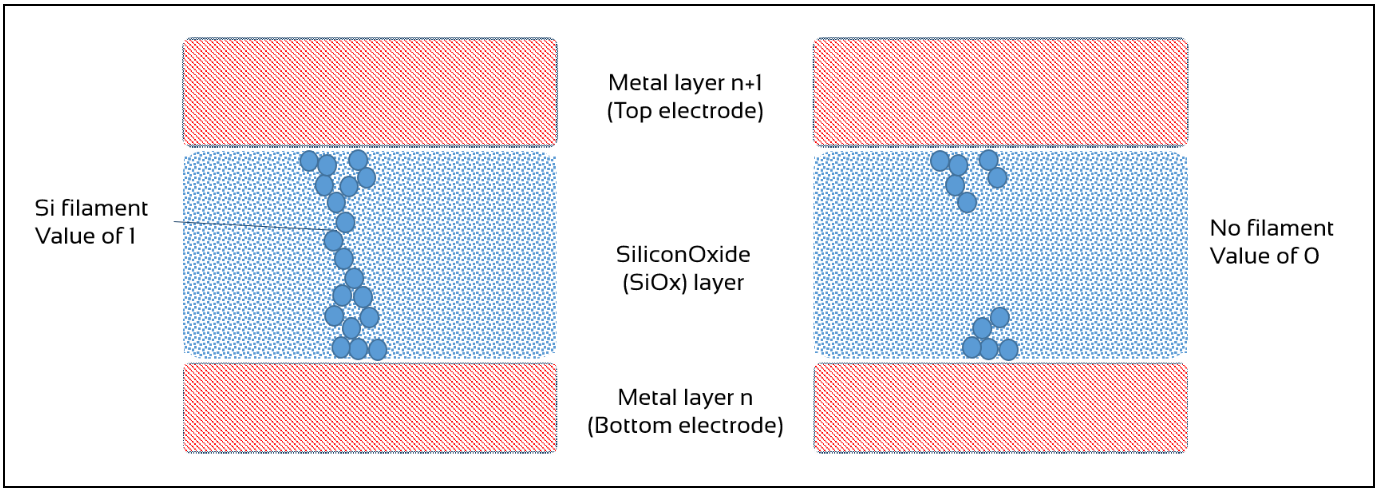
i) Through interface switching, which changes the resistivity of the entire layer between the electrodes or

ii) By creating a filament that connects the two electrodes.

WBT uses the latter.

The technology WBT is developing is based on the forming of a conductive channel between the two metal electrodes of a ReRAM cell. These electrodes are typically made of metals, such as titanium, tungsten, aluminium or copper. The conductive channel is formed inside a non-conductive SiOx layer.

Figure 1: Cell switching by forming and breaking a silicon filament in a SiOx switching layer



Source: Pitt Street Research

SiO_x has typically been used as an insulating component in semiconductor manufacturing. However, by applying a certain voltage to one of the electrodes, a switchable conductive pathway of silicon nanowires (filament) can be formed within the SiOx layer (Figure 1). In this high-conductivity, low-resistance state, the cell value is 1. By subsequently applying a reverse voltage to the electrode, the filament can be broken down again, effectively switching the memory cell back to the original state of 0.

The actual filament is formed as the applied electrical voltage strips away some of the oxygen atoms in the SiOx layer, leaving the silicon atoms to cluster and form a conductive silicon pathway to the other electrode. The filament is ~5 nanometer (nm) to 7nm in diameter.

WBT uses SiOx in its ReRAM cells, a material that is understood well by the semiconductor industry and has been used in chip manufacturing for decades. We believe that the industry's familiarity with SiOx is a key factor in driving the adoption of WBT's technology among both semiconductor design houses and foundries.

ReRAM's technical parameters validate its commercial use

The endurance and retention levels demonstrated by WBT's technology open up many commercial opportunities

The key parameters for any non-volatile memory are retention and endurance. As demonstrated in the tests conducted by WBT's research partner Leti in May 2019, the company's ReRAM technology is at the forefront of the ReRAM market. The tests demonstrated data retention of over 10 years at 130-150°C, and endurance of a million cycles. Notably, these endurance levels are significantly higher than today's state-of-the-art Flash memory technologies.

Moreover, the retention levels that were achieved at these high temperatures have broadened the scope of potential commercial applications wherein WBT's technology can be used, including the most notable addressable market of electric vehicles.

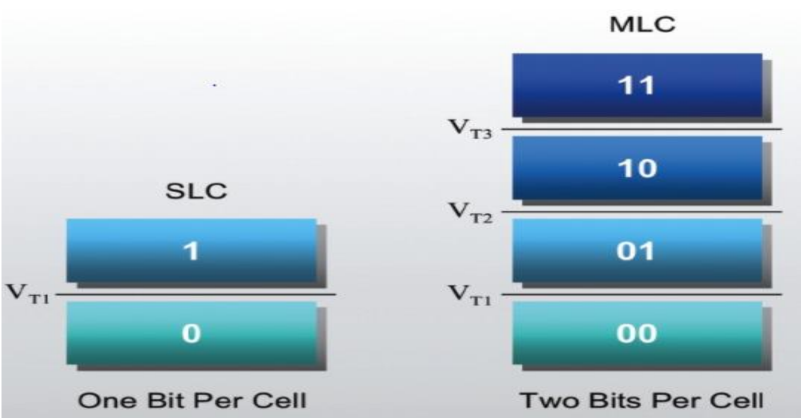
Appendix II – MLC technology

MLC technology: Putting more data in the same cell is another way to increase density

Traditionally, memory cells had two possible states, 1 and 0, and therefore could contain 1 bit of data. These cells are termed as single-level cells (SLC). However, now MLCs are available wherein the stored charge can be a variety of values and 2 bits of data can be stored in a single cell (Figure 2). MLC technology thus allows more data per unit of area to be packed on to a chip compared to SLC.

Typically, the cycling endurance and reliability required in end-user applications determine the appropriate storage technology to be used. SLCs have lower power consumption and therefore a longer lifespan compared to MLC (~100,000 cycles for SLC versus ~10,000 for MLC). Owing to higher reliability and faster speeds, SLC can be found in high-end storage applications, including data centre storage. However, MLCs are less expensive to manufacture per unit of storage and this makes MLC Flash the most used Flash, especially in consumer electronics such as mobile phones, cameras and tablets.

Figure 2: Relative voltage levels for SLC and MLC



Source: Pitt Street Research

Appendix III – Analyst Certification

Marc Kennis, lead analyst on this report, has been covering the semiconductor sector as an analyst since 1997.

- Marc obtained an MSc in Economics from Tilburg University, Netherlands, in 1996 and a post graduate degree in investment analysis in 2001.
- Since 1996, he has worked for a variety of brokers and banks in the Netherlands, including ING and Rabobank, where his main focus has been on the technology sector, including the semiconductor sector.
- After moving to Sydney in 2014, he worked for several Sydney-based brokers before setting up TMT Analytics Pty Ltd, an issuer-sponsored equity research firm.
- In July 2016, with Stuart Roberts, Marc co-founded Pitt Street Research Pty Ltd, which provides issuer-sponsored research on ASX-listed companies across the entire market, including technology companies.

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